**Introduction**

In this lab, minimization and the properties of a multiple input, multiple output circuit was explored. Among the properties demonstrated are logic circuit hazards.

In lab 2, this circuit diagram was given:



**Preliminary Work**

1) To find the functionality of the circuit we created a truth table, as show below.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | X1 | X2 | X3 | X4 | X5 | X6 | X7 | F1 | F2 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

From the truth table we obtained a sum of products (SOP) expression of the circuit:

A’BC+ AB’C’+ ABC’+ ABC

Then we minimized the expression:

BC(A+A’)+AC’(B+B’)

BC+AC’

2) Then we drew the minimized circuit:



3) Then we created a truth table for the minimized circuit:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | C’ | AC’ | BC | AC’+BC | F1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

4) Then we used a KMAP to find any new sets that would avoid hazards

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| \ |  | AB |  |  |  |
|  | \ | 00 | 01 | 11 | 10 |
| C | 0 |  |  | 1 | 1 |
|  | 1 |  | 1 | 1 |  |

5) Then we drew the circuit with the new set AB included



6) Then I created a wire list

U1 = SN74LS04 (NOT)

U2 = SN74LS08 (AND)

U3 = SN74LS02 (NOR)

VCC 🡪 U1-14, U2-14, U3-14

GND 🡪 U1-7, U2-7, U3-7

A 🡪 U2-1, U2-9

B 🡪 U2-4, U2-10

C 🡪 U1-1, U2-5

U1-2(X1) 🡪U2-2

U2-3 (Y2) 🡪 U3-2

U2-6 (Y3) 🡪 U3-3

U2-11 (Y2) 🡪 U3-4

U3-1 (Z4) 🡪 U1-3

U1-4 (F) 🡪 LED

**Lab Work**

Build the hazardous circuit and connect it to the function generator and oscilloscope to see results. Then construct the hazard-free circuit and check results again.

**Results**

I was not able to build the hazardous circuit.

**Observations and Conclusions**

I tested my chips separately to pinpoint the error. The NOT chip appeared to be the convict, but after using the spare chip and a friend’s working chip it may not have been the problem after all.

**Circuit Modification**

We found that the XOR chip is different from the chips we’ve been use to. The output gate is 1 and the input gates are 2 and 3. Throughout the lab I placed the output wire in different spots to test parts of the circuit.